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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,658	04/14/2004	Kohei Oikawa	251862US2S	4967

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,658	OIKAWA, KOHEI	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/1/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-17 have been submitted for examination
- Claims 1-17 have been rejected

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Shinoda et al. US patent no. 4817052 (Hereinafter Shinoda).

2. In regard to claim 1, Shinoda teaches:

- A semiconductor memory device comprising:

(Note: FIG. 1 in Shinoda)

- a memory array including at least a first area and a second area, which stores cell data;

(Note: FIG.1, reference characters (M-ART2, M-ARY4) and (M-ARY1, M-ARY3) in Shinoda)

- a data input circuit located closer to the first area than the second area, to which the cell data is input;

(Note: FIG. 1, reference character (DOB) in Shinoda)

- an error correction circuit which generates parity data for error correction from the cell data input to the data input circuit; and

(Note: FIG. 1, reference character (ECC) in Shinoda)

- a control circuit which stores the parity data in the first area.

(Note: FIG. 1, reference character (CONTROL CKT) in Shinoda)

3. In regard to claim 2, Shinoda teaches:

- The semiconductor memory device according to claim 1, wherein the memory array includes a first memory unit and a second memory unit having the first area and the second area, respectively.

(Note: FIG.1, reference characters (M-ART1, M-ARY2) and (M-ARY3, M-ARY4) in Shinoda)

4. In regard to claim 3, Shinoda teaches:

- The semiconductor memory device according to claim 1, wherein the memory array includes a first data line connected to the first area and a second data line connected to the second area.

(Note: FIG. 1, the address lines connected to the Y DECODER and the (X DECODER(S) and the SENSE AMPLIFIER(S)

5. In regard to claim 4, Shinoda teaches:

- The semiconductor memory device according to claim 3, further comprising a switch between the first data line and the second data line.

(Note: FIG. 1, reference characters (MPX1-MXP4 in Shinoda)

6. In regard to claim 5, Shinoda teaches:

The semiconductor memory device according to

claim 1, wherein the memory array includes a common data line connected to both the first area and the second area.

(Note: FIG. 1, output lines from the X DECODER(S))

7. In regard to claim 6, Shinoda teaches:

- A semiconductor memory device comprising:

(Note: FIG. 1 in Shinoda)

- a memory array including at least a first area and a second area;

(Note: FIG.1, reference characters (M-ART2, M-ARY4) and (M-ARY1, M-ARY3) in Shinoda)

- a data input circuit located closer to the first area than the second area, cell data to be stored in the memory array being input to the data input circuit;

(Note: FIG. 1, reference character (DOB) in Shinoda)

- an error correction circuit which generates parity data for error correction from the cell data input to the data input circuit; and

(Note: FIG. 1, reference character (ECC) in Shinoda)

- a control circuit which stores the parity data in the first area and store the cell data in the second area.

(Note: FIG. 5 and col.'s 15-18, (TABLE 3) in Shinoda)

8. In regard to claim 7, Shinoda teaches:

- The semiconductor memory device according to claim 6, wherein the control circuit stores both the parity data and the cell data in the first area and store the cell data not including the parity data in the second area.

(Note: FIG. 5 and col.'s 15-18, (TABLE 3) in Shinoda)

9. Claim 8 is rejected for the same reasons as per claim 2.

10. In regard to claim 9, Shinoda teaches:

- The semiconductor memory device according to claim 8, wherein the first memory unit has a first data line connected to the first area and a second data line connected to the second area, and the second memory unit has a first data line connected to the first area and a second data line connected to the second area.

(Note: FIG. 1, the address lines connected to the Y DECODER and the (X DECODER(S) and the SENSE AMPLIFIER(S))

11. Claim 10 is rejected for the same reasons as per claim 4.

12. Claim 11 is rejected for the same reasons as per claim 5.

13. In regard to claim 12, Shinoda teaches:

- The semiconductor memory device according to claim 1, wherein the memory array includes at least a first memory unit and a second memory unit each having the first area and the second area, and the semiconductor memory device further comprises a switching circuit

which stores the parity data in the first area of one of the first memory unit and the second memory unit.

(Note: FIG. 5 and col.'s 15-18, (TABLE 3) in Shinoda)

14. In regard to claim 13, Shinoda teaches:

- The semiconductor memory device according to claim 1, further comprising a data compensating circuit which error-corrects the cell data stored in the memory array using the parity data stored in the first area.

(Note: FIG. 5. in Shinoda)

15. In regard to claim 14, Shinoda teaches:

- The semiconductor memory device according to claim 1, wherein a size of the first area is equal to or smaller than that of the second area.

(Note: FIG. 1, reference characters (M-ARY1)-(M-ARY4) in Shinoda)

16. Claim 15 is rejected for the same reasons as per claim 12.

17. Claim 16 is rejected for the same reasons as per claim 13.

18. Claim 17 is rejected for the same reasons as per claim 14.

Conclusion

19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Barth Jr. et al. US patent no. 5134616 teaches dynamic RAM with on-chip ECC and optimized bit and word redundancy.

- Fifield et al. US patent no. 5638385 teaches fast check bit write for a semiconductor memory.
- Sugiyama et al. patent no. 5568609 teaches data processing system with path disconnection and memory access failure recognition.
- Sugiyama et al. US patent no. 5548743 teaches data processing system with duplex common memory having physical and logical path disconnection upon failure.
- Fujioka et al. US publication 2003/0106010 teaches memory circuit having parity cell array.
- Egawa US patent no. 6289481 teaches multi-value type semiconductor memory device and its defect removal method.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

12/14/06

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